THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 26

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

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Ex parte ALLEN P. JENSEN and MICHAEL T. VANOVER

_____

Appeal No. 95-0933
Application 08/032,764[1]

_____

ON BRIEF

_____

Before THOMAS, KRASS and FLEMING, ***Administrative Patent Judges***.

FLEMING, ***Administrative Patent Judge***.

DECISION ON APPEAL

This is a decision on appeal from the final rejection of claims 1 through 17, all of the claims pending in the

[1]Application for patent filed March 16, 1993. According to appellants this application is a continuation of application 07/614,353, filed November 15, 1990.

application.

The invention relates generally to a computer designed to parallel execute arithmetic and logical operations on packed data. In particular, Appellants disclose on page 3 that

Figure 2

shows a diagram of three operands 210, 220 and 230 packed into a single 32 bit word 200. Appellants further disclose that the 32 bit word 200 includes buffer bits 240, 250 that are placed between the operands.

Independent claims 1 is reproduced as follows:

> 1. Method of processing a plurality of multidigit operands in parallel comprising the steps of:
>
> a) packing the multidigit operands into a first word with at least one buffer bit between each multidigit operand; and
>
> b) performing arithmetic operations on the first packed word with a second word, thereby providing a processed packed word.

The reference relied on by the Examiner is as follows:

Bertrand	4,963,867	Oct. 16, 1990

Claims 1 through 17 stand rejected under 35 U.S.C. § 102

as being anticipated by Bertrand.

Rather than repeat the arguments of Appellants or the Examiner, we make reference to the briefs and the answers for the

details thereof. We note that the claims that are before us are

found in the appendix[2] provided in the supplemental reply brief,

filed January 13, 1998.

OPINION

After a careful review of the evidence before us, we do not agree with the Examiner that the claims are anticipated under 35 U.S.C. § 102 by Bertrand.

[2]In this supplemental reply brief, Appellants provide the appealed claims in an attached appendix. The Examiner stated in a letter, mailed January 30, 1998, that the supplemental reply brief has been entered and considered but no further response by the Examiner is deemed necessary. We note that the Examiner's communication did not object to these claims. We will take the Examiner's silence as the Examiner's acceptance that these claims are the proper claims for our consideration for this appeal.

It is axiomatic that anticipation of a claim under § 102 can be found only if the prior art reference discloses every element of the claim. ***See In re King***, 801 F.2d 1324, 1326, 231 USPQ 136, 138, (Fed. Cir. 1986) and ***Lindemann Maschinenfabrik GMBH v. American Hoist & Derrick Co***., 730 F.2d 1452, 1458, 221 USPQ 481, 485, (Fed. Cir. 1984).

Appellants argue on page 6 of the brief that Appellants' claims recite packing multidigit operands into a packed word with at least one buffer bit between each of the multidigit operands. Appellants argue on page 7 of the brief that buffer bit is defined on page 3, line 33, through page 4, line 10, as a bit of data stored between operands to prevent the propagation of a bit of data from flowing into bits of another operand during
arithmetic or logical operations. Appellants then argue that Bertrand fails to teach the buffer bit stored between operands to prevent the propagation of a bit of data from flowing into bits of another operand during arithmetic or logical operations as claimed.

When interpreting a claim, words of the claim are

generally given their ordinary and customary meaning, unless it appears from the specification or the file history that they were used differently by the inventor. ***Carroll Touch, Inc. v. Electro Mechanical Sys., Inc.*** 15 F.3d 1573, 1577, 27 USPQ2d 1836, 1840 (Fed. Cir. 1993). Thus, we find that Appellants' claimed term, buffer bit, must be given the meaning of a bit of data stored between operands to prevent the propagation of a bit of data from flowing into bits of another operand during arithmetic or logical operations.

On page 10 of the Examiner's answer, the Examiner states that the Examiner agrees with the Appellant that Bertrand fails to teach the claimed buffer bit. Upon our review of Bertrand, we find that Bertrand fails to teach the buffer bit stored between operands to prevent the propagation of a bit of data from

flowing into bits of another operand during arithmetic or logical operations as claimed.

In view of the foregoing, the decision of the Examiner

rejecting claims 1 through 17 is reversed.

REVERSED

JAMES D. THOMAS Administrative Patent Judge	)	
ERROL A. KRASS Administrative Patent Judge	)	BOARD OF PATENT APPEALS AND INTERFERENCES
MICHAEL R. FLEMING Administrative Patent Judge	)	

vsh

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